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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,703	09/28/2006	Shinichi Abe	KY-5510	1765

7590 02/21/2008

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
02/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,703	ABE ET AL.	
	Examiner	Art Unit	
	Jean B. Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9-28-06.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 September 2006 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 9-28-06.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure. *The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words.* It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

It is suggested not to use the word “comprises” in the abstract.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 - 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Vu et al. (US Patent Number 6,654,066).

5. Regarding claim 1, Vu et al. discloses a D/A converter circuit (fig. 2), which includes a first current mirror circuit (col. 2, lines 5 – 20; fig. 2) having a plurality of output side transistors provided correspondingly to digits of data to be converted and generates an analog current by obtaining in at least one of the output side transistors a current corresponding to weight of digit of the data, comprising: a second current mirror circuit (col. 2, lines 5 – 25; fig. 2) connected on an upstream or down stream side of at least one of the output side transistors corresponding to lower digit of the data, wherein operating current ratio of the output side transistor of the second current mirror circuit with respect to an input side transistor thereof is set to n:1 (where n is a positive integer) and the analog current is generated by obtaining a current corresponding to weight of digit, which is smaller than 1, on the output side transistor of the second current mirror circuit (fig. 2).

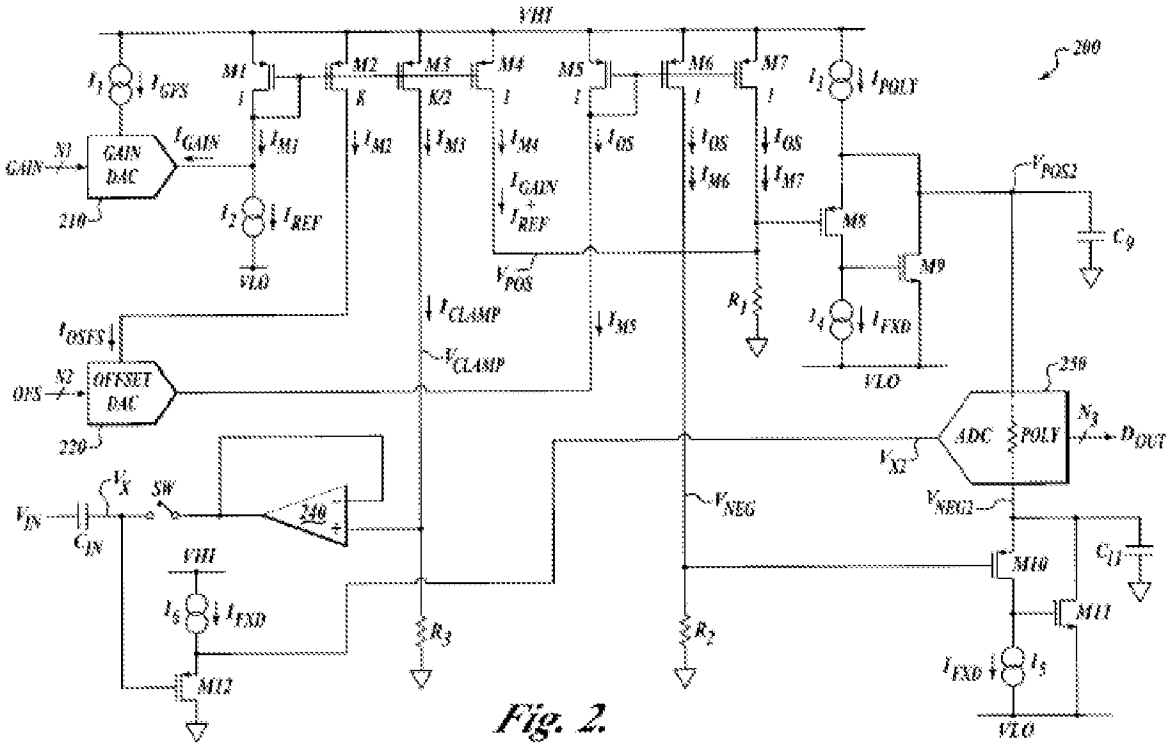

Fig. 2.

6. Regarding claim 2, Vu et al. discloses a D/A converter circuit (fig. 2) , wherein the current corresponding to the weight of a digit smaller than 1 is outputted to the output terminal of the D/A converter circuit as corresponding to at least one of lower digits of the data to be converted (fig. 2).

7. Regarding claim 3, Vu et al. discloses a D/A converter circuit (fig. 2), further comprising a constant bias circuit, wherein voltages of the output electrodes of the input

side transistor and the output side transistors of the second current mirror circuit are set to a predetermined constant voltage by the constant voltage bias circuit (fig. 2).

8. Regarding claim 4, Vu et al. discloses a D/A converter circuit (fig. 2) wherein the constant voltage bias circuit includes a constant voltage circuit and a plurality of transistors which are connected in series with the input side transistor and the output side transistors of the second current mirror circuit, respectively, the voltage the output electrodes are set to the constant voltage by setting gates or bases of the plurality of the transistors in series with the input and output side transistors to a predetermined constant voltage by the constant voltage circuit (fig. 2).

9. Regarding claim 5, Vu et al. discloses a D/A converter circuit (fig. 2), wherein the data to be converted is m-bit data, m/2 is used as the digit having weight of 1 when m is an even number, a center digit is used as the digit having weight of 1 when m is an odd number, the second current mirror circuit is provided for each of digits having weights smaller than 1 and the n is selected correspondingly to the digit having weights smaller than 1, respectively (fig. 2).

10. Regarding claim 6, Vu et al. discloses a D/A converter circuit (fig. 2) , wherein the input side transistor and the output side transistors of the second current mirror circuit and the plurality of the transistors connected in series with the input and output side transistors are MOS transistors, respectively, and values of the currents, which are obtained by dividing the operating currents of the second current mirror circuit by powers of 2, are distributed to the output side transistors of the second current mirror circuit and outputted to the output terminals, respectively (fig. 2).

11. Regarding claim 7, Vu et al. discloses a D/A converter circuit (fig. 2) wherein the input side transistor and the output side transistors of the second current mirror circuit and the plurality of the transistors connected in series with the input and output side transistors are MOS transistors, respectively, and the constant voltage bias circuit includes a voltage follower for connecting the output electrode of the output side transistor of the second current mirror circuit to the output electrodes of the input side transistor (fig. 2).

12. Regarding claim 8, Vu et al. discloses a D/A converter circuit wherein the data to be converted is 8 bits or more (fig. 2).

13. Regarding claim 9, Vu et al. discloses a D/A converter circuit (fig. 2) wherein the data to be converted is a gamma corrected display data of 8 bits or more (fig. 2).

14. Regarding claim 10, Vu et al. discloses an organic EL drive circuit (fig. 2) wherein the data to be converted in claim 1 is a display data and an organic EL element is driven by an output current of a D/A converter circuit (fig. 2).

15. Regarding claim 11, Vu et al. discloses an organic EL drive circuit (fig. 2) comprising a D/A converter circuit and a current source driven by an output current of the D/A converter circuit, for driving an organic EL element, where the data to be converted (fig. 2).

16. Regarding claim 12, Vu et al. discloses an organic EL display device comprising an organic EL drive circuit (fig. 2).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (see PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jean B Jeanglaude/
Primary Examiner, Art Unit 2819